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AMENDEMENTS TO THE CLAIMS

Claims 1-8 are currently pending in the application.

Please cancel claims 1-8 as shown below.

Please add claims 9-12 as shown below.

This listing of claims 1-12 will replace all prior versions, and listings, of claims in the application:

1.-8. (Cancelled)

9. (NEW) An active matrix array device, comprising:

a substrate;

an array of individually addressable matrix elements carried on said substrate;

a set of address conductors connected to said array of matrix elements and carried on said substrate, said set of address conductors being arranged in a series of groups with each group including successive address conductors; and

an addressing circuit including

a multiplexing circuit integrated on the substrate and connected to the set of address conductors, said multiplexing circuit including a plurality of signal bus lines, said multiplexing circuit being arranged to couple sequentially each group of said set of address conductors to said plurality of signal bus lines with each address conductor in a group being coupled to a respective one of said signal bus lines, and

a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein each individual signal processing circuit associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on said substrate.

10. (New) The active matrix array device of claim 9, wherein said signal processing circuits are arranged in series in a line parallel to said multiplexing circuit.

11. (NEW) The active matrix array device of claim 9, wherein a first subset of said signal processing circuits are arranged in a first row and a second subset of said

signal processing circuits are arranged in a second row and offset from the first row in a brick-like fashion.

12. (New) The active matrix array device of claim 9, wherein the order in which said signal processing circuit circuits are arranged physically on said substrate is different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected.